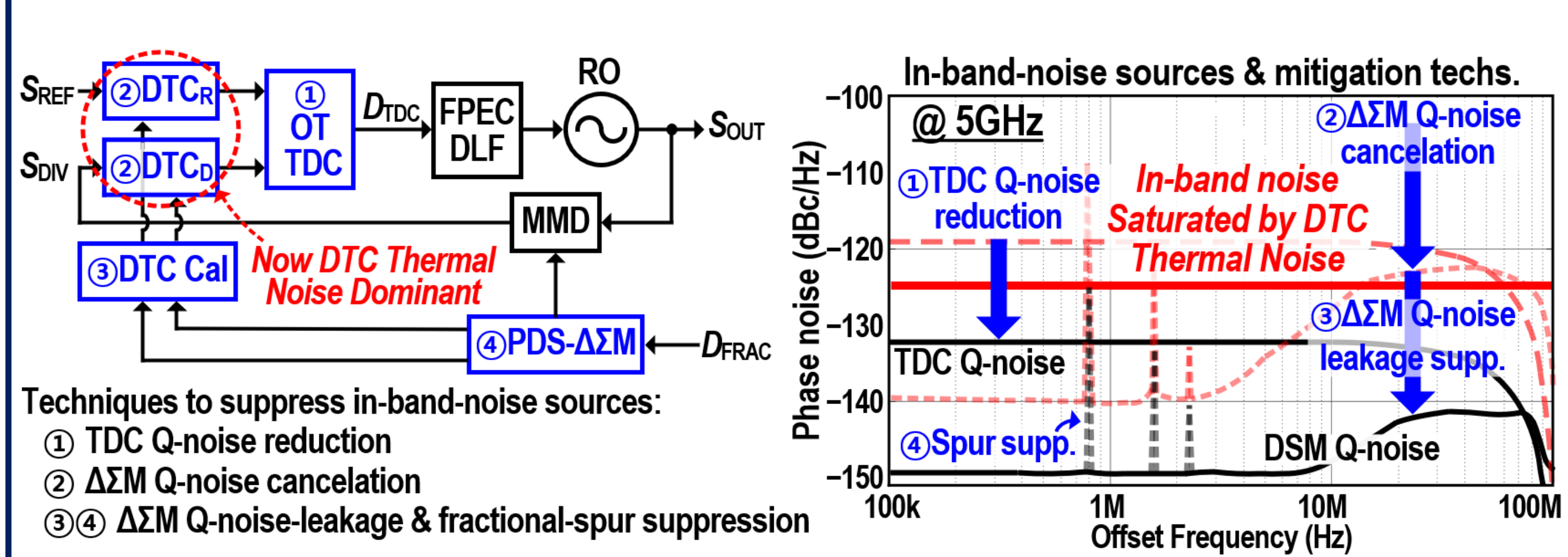




# A 188fs<sub>rms</sub>-Jitter and -243dB-FoM<sub>jitter</sub> 5.2GHz-Ring-DCO-Based Fractional-N Digital PLL with a 1/8 DTC-Range Reduction Technique

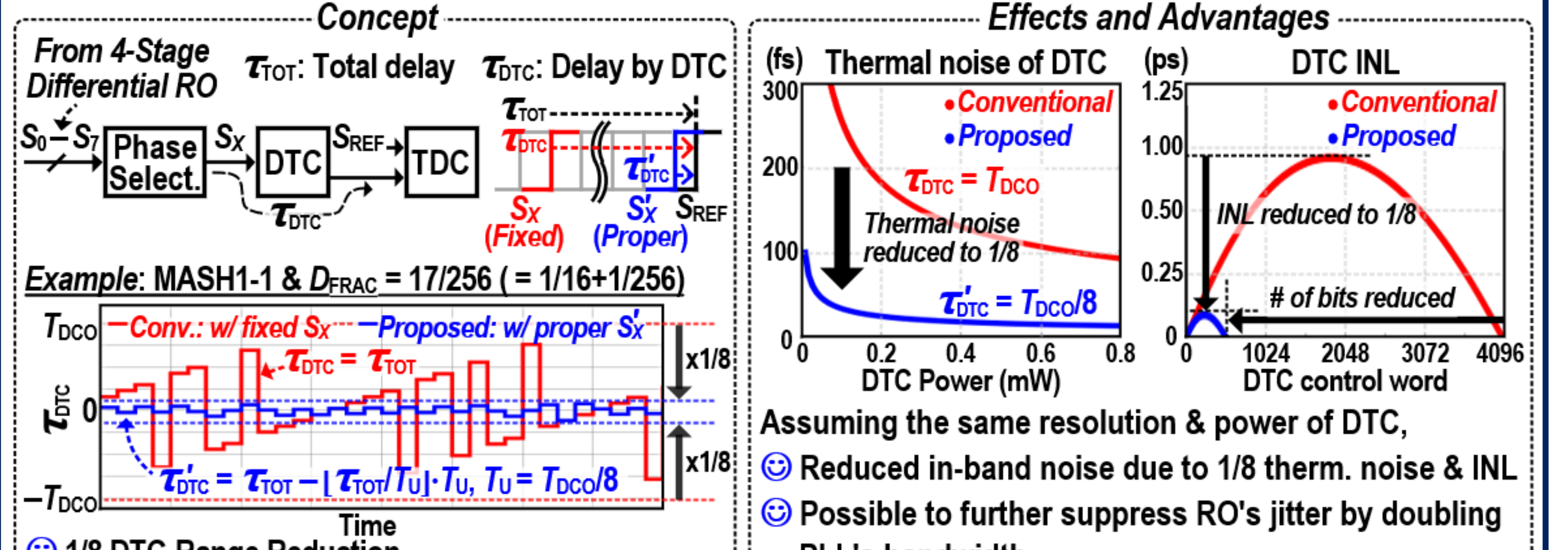
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## Introduction: Design of low-jitter RO-DPLL



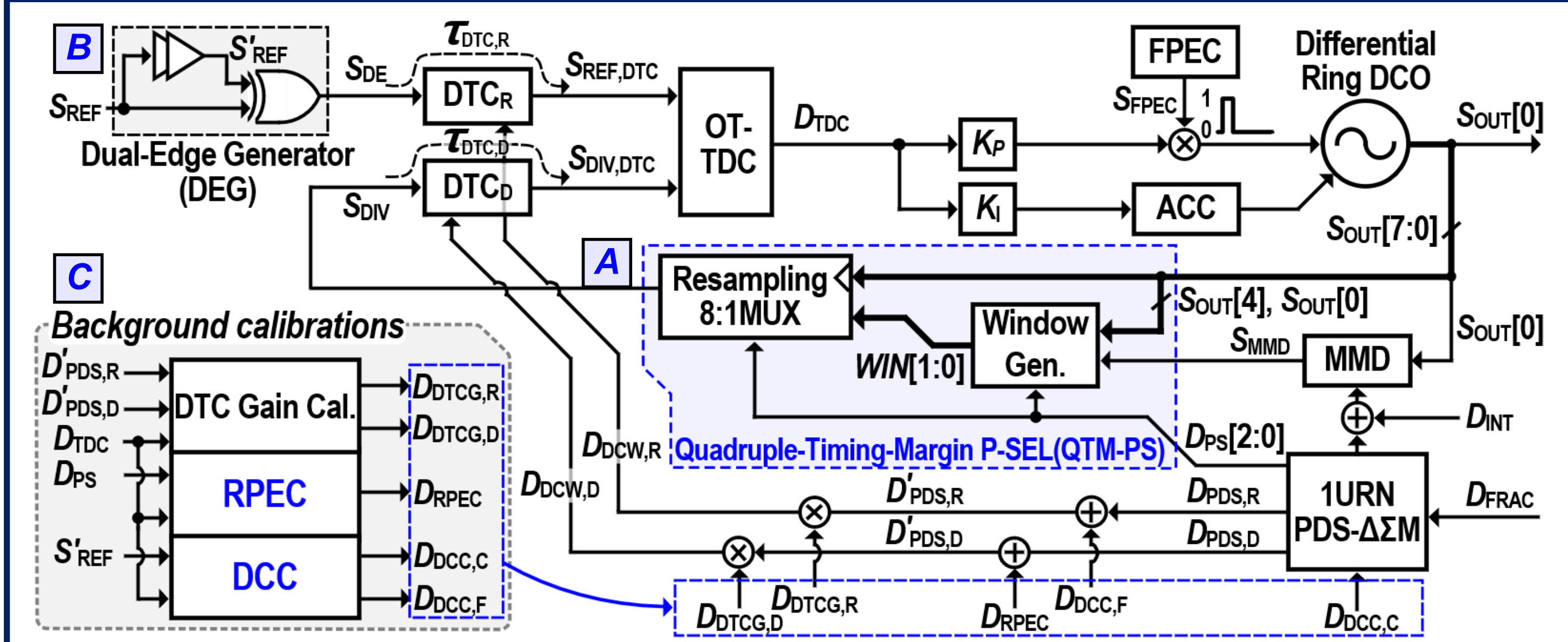
- Common strategy of design of low jitter RO-DPLL:  
To maximize the PLL bandwidth for reduction of phase noise of ring osc.  
→ Essential to mitigate major in-band noise sources of RO-DPLL (i.e. TDC Quantization -noise (QN),  $\Delta\Sigma$  QN, DTC thermal noise)
- Recent RO-DPLL [2] achieved sub-400 fs<sub>rms</sub> @ 5GHz with prior tech. ①-③  
→ But, still worse than practical LC-osc. based analog PLL  
→ Next dominant in-band noise source: Thermal noise of the DTC

## Concept & Effect of DTC range reduction



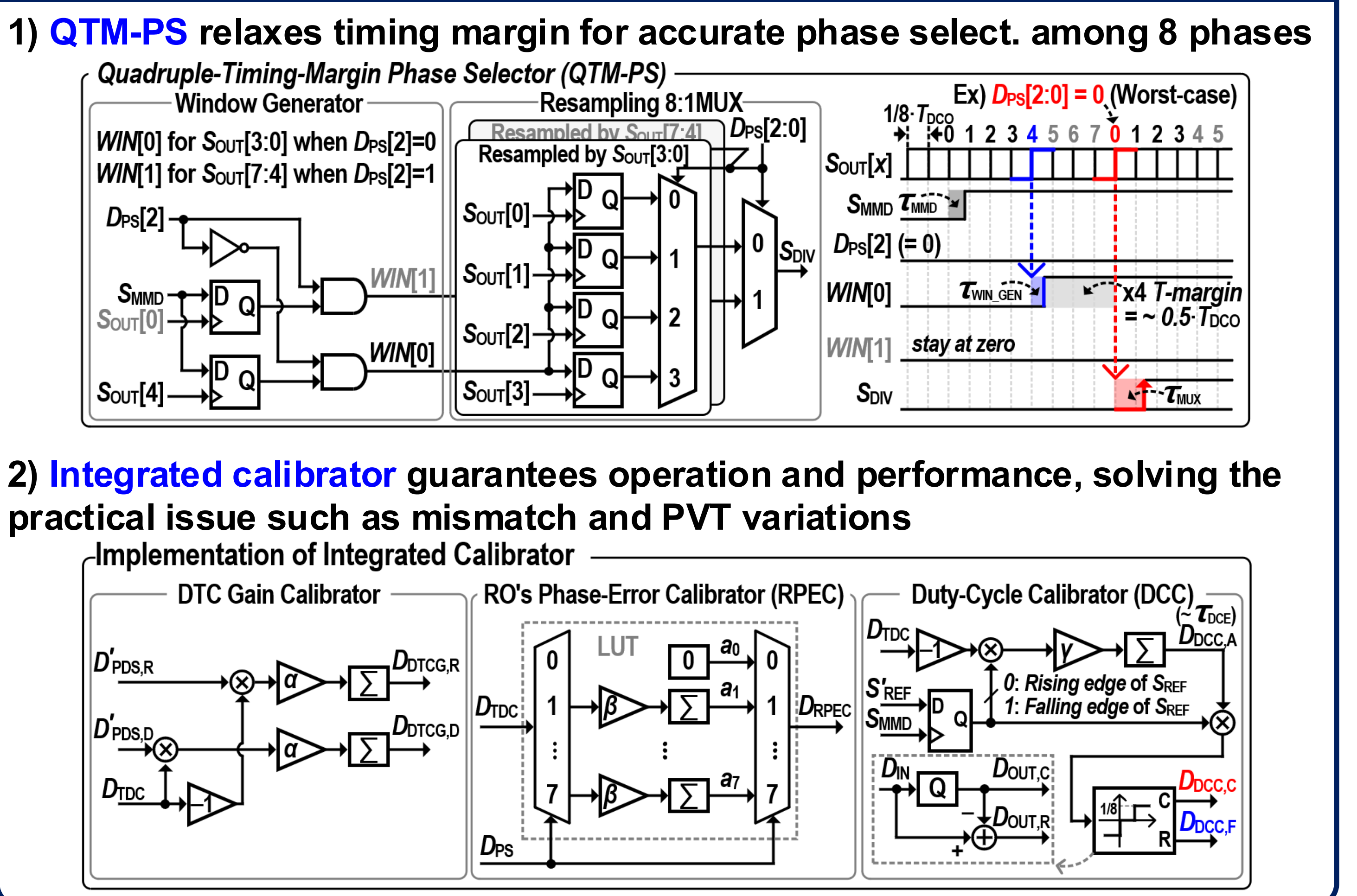
- Brute force way to reduce the thermal noise of the DTC:  
To reduce the dynamic range of the DTC
- With naturally available multiple phases of the RO (i.e.,  $S_0$  to  $S_7$  spaced by  $1/8 T_{DCO}$ , for 4-stage RO), dynamic range of the DTC can be reduced to 1/8
- Reduced thermal noise of DTC & better cancellation of  $\Delta\Sigma$  QN help the in-band noise of the PLL to decrease significantly.

## Overall Architecture w. DTC range reduction

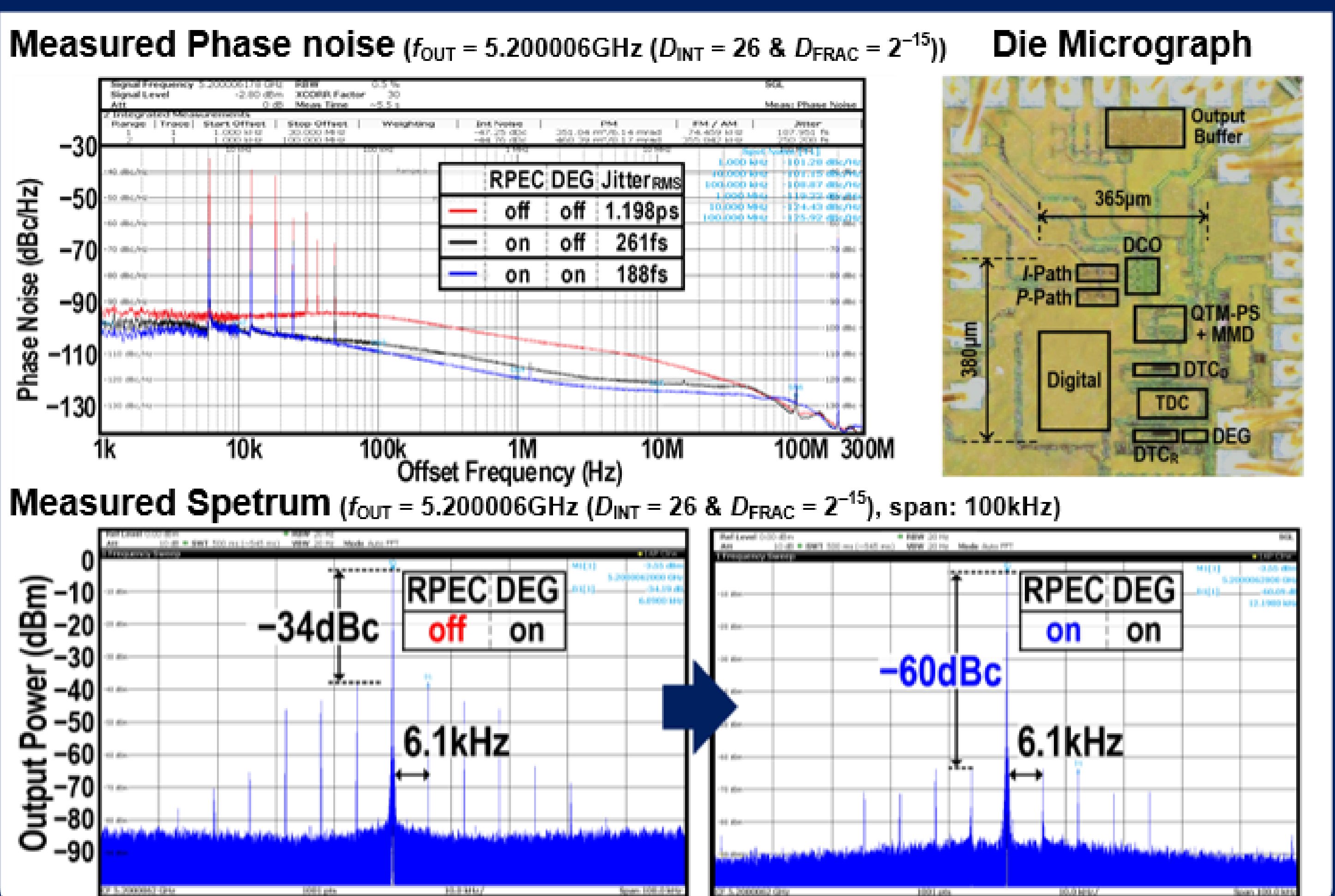


- Quadruple-timing-margin phase-selector (QTM-PS) implements the 1/8 DTC range reduction along with PDS- $\Delta\Sigma$  ... A
- Dual-edge generator (DEG) doubles the bandwidth of the PLL to further reduce the jitter of the RO ... B
- Integrated calibrator guarantees the stable operation of the QTM-PS and the DEG ... C

## QTM-PS & Integrated calibrator



## Measurement Results



## Performance Comparison

Reference	This Work	ISSCC'21 H. Park	CICC'21 A. Elmallah	TCAS-I'21 B. Liu	ISSCC'20 T. Seong	JSSC'19 A. Santiccioli
Architecture	DPLL	DPLL	DPLL	MDLL	DPLL	MDLL
Technology	65nm	65nm	65nm	65nm	65nm	65nm
$f_{OUT}$ (GHz)	5.2 (4.4 to 5.4)	5.3 (5.2 to 6.0)	3.26	1.0 (0.8 to 1.6)	5.5 (4.5 to 6.0)	1.65 (1.6 to 3.0)
Freq. resolution (kHz)	6.1	3.1	11.7	6.1	3.1	1960
$f_{REF}$ (MHz)	100	100	96	100	100	100
Worst frac. spur (dBc)	-60	-63	-51	-60	-58	-52
Ref. spur (dBc)	-64	-77	NA	-64.5	NA	-56
rms jitter (fs)	188 (1k to 30M)	365 (10k to 30M)	405 (1k to 30M)	560 (10k to 40M)	648 (1k to 30M)	397 (30k to 30M)
*PN@1MHz (dBc/Hz)	-133.4	-128.8	-129.3	-125.44	-124.9	-122.4
Power (mW)	15.67	9.27	11.7	1.85	9.88	2.5
**FoM <sub>jitter</sub> (dB)	-242.6	-239.1	-237.2	-242.3	-233.8	-244.0
***FoM <sub>jitter,N</sub> (dB)	-259.7	-256.3	-252.5	-252.3	-251.2	-256.2
Area (mm <sup>2</sup> )	0.139	0.146	0.134	0.126	0.108	0.0275

\*Normalized to 1GHz, \*\*FoM<sub>jitter</sub> (dB) = 10log<sub>10</sub>[(Jitter<sub>rms</sub>/1s)<sup>2</sup> (P<sub>dc</sub>/1mW)], \*\*\*FoM<sub>jitter,N</sub> (dB) = FoM<sub>jitter</sub> (dB) + 10log(f<sub>REF</sub>/f<sub>OUT</sub>)

☺ The proposed RO-DPLL achieved the RMS jitter of 188 fs and FoM<sub>JIT</sub> of -243dB, which is the best among the state-of-the-art fractional-N RO-PLLs

References [1] T. Seong et al., JSSC, vol. 54, no. 9, pp. 2501-2512, Sept. 2019 [2] H. Park et al., ISSCC, pp. 442-443, Feb. 2021. [3] A. Santiccioli et al., et al., JSSC, vol. 54, no. 11, pp. 3149-3160, Nov. 2019 [4] W. Wu et al., ISSCC, pp. 444-446, Feb. 2021.

Acknowledgement The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEAC), Korea.